We Claim:

1. A method for producing a vertical semiconductor transistor component, the method which comprises:

producing a series of layers on a substrate such that the series of layers includes layers of different electrical conductivities;

forming a statistical mask with statistically distributed mask structures over the series of layers;

forming pillar structures from the series of layers by using the statistical mask such that the pillar structures are electrically connected with one another at bases of the pillar structures for realizing a first electrical contact;

producing insulation layers on circumferential walls of the pillar structures;

depositing an electrically conductive material between the pillar structures provided with the insulation layers such that the electrically conductive material forms a second electrical contact; and

depositing an electrically conductive contact material for realizing a third electrical contact such that the

electrically conductive contact material electrically contacts capping regions of the pillar structures.

2. The method according to claim 1, which comprises producing the series of layers by using a selective n^+pn^+ epitaxial build-up process.

3. The method according to claim 1, which comprises producing the series of layers by using a selective p^+np^+ epitaxial build-up process.

4. The method according to claim 1, which comprises producing the series of layers by depositing alternating semiconductor layers and tunnel insulation layers such that respective layer thicknesses of the tunnel insulation layers are less than 5 nm.

5. The method according to claim 4, which comprises:

depositing silicon layers as the semiconductor layers; and

performing a lateral, self-limiting oxidation step for producing silicon pillar structure cores of reduced lateral dimensions subsequent to forming the pillar structures.

6. The method according to claim 1, which comprises setting a number of the pillar structures to a desired value by using a mask selection step.

7. The method according to claim 1, which comprises setting a number of the pillar structures to a value between 100 and 200 by using a mask selection step.

8. The method according to claim 1, which comprises producing the statistical mask by depositing, with a chemical vapor deposition process, a material on a surface disposed above the series of layers wherein the material forms seeds when deposited on the surface.

9. The method according to claim 1, which comprises producing the statistical mask by depositing, with a chemical vapor deposition process, a continuous layer on a surface disposed above the series of layers and by subsequently performing an annealing step for disintegrating the continuous layer into individual seeds.

10. A vertical semiconductor transistor component, comprising:

a substrate;

vertical pillar structures disposed on said substrate, said vertical pillar structures having respective base sides, circumferential wall regions, and capping sides, said vertical pillar structures being statistically distributed over said substrate;

a first common electrical contact electrically connected to said vertical pillar structures at said base sides;

said vertical pillar structures defining a vertical direction and having respective layer zones with respective different conductivities disposed along the vertical direction;

said vertical pillar structures including respective insulation layers provided at said circumferential wall regions such that said vertical pillar structures are circumferentially insulated;

an electrically conductive material deposited between said vertical pillar structures, said electrically conductive material forming a second electrical contact; and

a third common electrical contact electrically connected to said vertical pillar structures at said capping sides.

11. The vertical semiconductor transistor component according to claim 10, wherein said vertical pillar structures are statistically distributed over said substrate in accordance with a statistical mask used for forming said vertical pillar structures.

12. The vertical semiconductor transistor component according to claim 10, wherein said vertical pillar structures include, as said layer zones, a n^+pn^+ layer series disposed along the vertical direction.

13. The vertical semiconductor transistor component according to claim 10, wherein said vertical pillar structures include, as said layer zones, a p^+np^+ layer series disposed along the vertical direction.

14. The vertical semiconductor transistor component according to claim 10, wherein said vertical pillar structures respectively include at least one tunnel insulation layer zone.

15. The vertical semiconductor transistor component according to claim 10, wherein:

said vertical pillar structures include, as said layer zones, at least two silicon core layer zones and a tunnel insulation

layer zone separating said at least two silicon core layer zones from one another; and

said at least two silicon core layer zones have respective silicon cores provided within said at least two silicon core layer zones, said silicon cores have lateral dimensions of less than 20 nm.

16. The vertical semiconductor transistor component according to claim 10, wherein between 100 and 200 of said vertical pillar structures are provided for the vertical semiconductor transistor component.